Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1-2 (Canceled)

A2

Claim 3 (Currently Amended): A method of manufacturing a field effect transistor ~~as recited in claim 1~~ having a semiconductor substrate with a main surface, comprising:

forming a conductive layer on the main surface via a dielectric film;

forming a gate electrode by etching the conductive layer using a mask formed thereon;

forming a source region and a drain region in the main surface; and

forming pocket regions in the semiconductor substrate by implanting ions using the mask,

wherein the mask has a width [[being]] less than a desired width necessary to ~~defined~~ define a gate length of the gate electrode, and the implanting ~~process~~ is carried out ~~so as to head~~ from an upward direction of the mask to the semiconductor substrate using the mask.

Claim 4 (Currently Amended): A method of manufacturing a [[filed]] field effect

transistor as recited in claim 3, wherein a dielectric spacer is formed on a side wall of the mask after the implanting, ~~process~~ and then the gate electrode is formed by etching the conductive layer using the mask with the dielectric spacer.

Claim 5 (Currently Amended): A method of manufacturing a field effect transistor as recited in claim 3, wherein the gate electrode is formed so as to have ~~expand~~ a greater width [[from]] at a top surface than at [[to]] a bottom surface, after the implanting ~~process~~.

A2 cont.

Claim 6 (Currently Amended): A method of manufacturing a field effect transistor as recited in claim 3 [[1]], wherein the pocket regions [[is]] are formed so as to underlie the gate electrode ~~pocket regions~~.

Claims 7-8 (Canceled)

Claim 9 (Currently Amended): A method of manufacturing a field effect transistor ~~as recited in claim 7~~ having a semiconductor substrate with a main surface, comprising:

forming a conductive layer on the main surface via a dielectric film;

forming a first mask on the conductive layer;

forming pocket regions in the semiconductor substrate by implanting ions using the first mask;

forming a gate electrode by etching the conductive layer using the first mask; and

forming a source region and a drain region in the main surface using the gate electrode as a mask,

wherein the pocket regions underlie the source and drain regions, and

wherein the first mask has a width [[being]] less than a desired width necessary to ~~defined~~ define a gate length of the gate electrode, and the implanting ~~process~~ is carried out ~~so as to head~~ from an upward direction of the first mask to the semiconductor substrate using the first mask.

A2 cont.

Claim 10 (Currently Amended): A method of manufacturing a field effect transistor as recited in claim 9, wherein a dielectric spacer is formed on a ~~sidewall~~ side wall of the first mask after the implanting, ~~process~~ and then the gate electrode is formed by etching the conductive layer using the first mask with the dielectric spacer.

Claim 11 (Currently Amended): A method of manufacturing a field effect transistor as recited in claim 9, wherein the gate electrode is formed so as to have ~~expand~~ a greater width [[from]] at a top surface [[to]] than at a bottom surface, after the implanting ~~process~~.

Claim 12 (Currently Amended): A method of manufacturing a field effect transistor as

recited in claim 9 [[7]], wherein the pocket regions are [[is]] formed so as to underlie the gate electrode[[,]] ~~pocket regions~~.

Claims 13-14 (Canceled)

A2 cont.

Claim 15 (Currently Amended): [[The]] A method of manufacturing a [[the]] field effect transistor ~~according to Claim 13~~ including a gate electrode formed on a semiconductor substrate, a pair of first impurity regions as a source and a drain formed on both sides of said gate electrode on said semiconductor substrate, and a pair of second impurity regions formed between said pair of first impurity regions that inhibits an expansion of a depletion layer from an impurity region of said pair of first impurity regions toward another impurity region of said pair of first impurity regions, said pair of second impurity regions being formed at an interval and exhibiting a conductive property different than that of said pair of first impurity regions, the method comprising:

forming a conductive layer for a gate electrode on said semiconductor substrate;

forming an etching mask for said gate electrode on said conductive layer;

removing unwanted portions of said conductive layer using photolithography; and

implanting an impurity in a predetermined region in said semiconductor substrate under said conductive layer by an ion implantation using said etching mask as a mask, to form said pair of second impurity regions,

wherein said etching mask has a width [[being]] less than a desired width

necessary to define ~~defining~~ a gate length of said gate electrode, and

wherein the impurities are ~~said ion is~~ implanted ~~at a right angle formed by a line heading~~ from an upward direction of said etching mask ~~to said inside of~~ into said semiconductor substrate at a right angle to [[and]] a line [[being]] that is vertical to [[said]] a surface of said semiconductor substrate.

A2 Cont.

Claim 16 (Currently Amended): The method of manufacturing [[the]] a field effect transistor according to claim [[Claim]] 15, wherein side walls are formed on said etching mask[[,]] after said implanting ~~ion implantation~~[[,]] to substantially ~~provide~~ correspond to said ~~desired~~ gate length of ~~width to~~ said gate electrode, and[[,]] by using said etching mask including ~~containing~~ said side walls as a resist mask, the unwanted ~~portion is~~ portions are removed from said conductive layer and said gate electrode having said ~~defining a predetermined~~ gate length is formed.

Claim 17 (Currently Amended): The method of manufacturing [[the]] a field effect transistor according to claim [[Claim]] 15, wherein[[,]] after said implanting ~~ion implantation~~ using said etching mask, ~~by performing etching processing using said etching mask as a resist mask~~[[,]] said gate electrode is formed as having a [[whose]] width that is increased along [[the]] a downward direction to ~~secure~~ have said ~~predetermined~~ gate length by an etching process using said etching mask as a resist mask.